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STAAS & HALSEY LLP
SUITE 700
1201 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER	
GERSTL, SHANE F	
ART UNIT	**PAPER NUMBER**
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/746,068	Applicant(s) ANDO, HISASHIGE
	Examiner Shane F Gerstl	Art Unit 2183

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *26 December 2001 and 26 December 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☒ Claim(s) *9,11 and 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 December 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. Claims 1-16 have been examined.

Papers Received

2. Receipt is acknowledged of foreign priority papers submitted, where the papers have been placed of record in the file.

Drawings

3. Figures 1-3 should be designated by a legend such as –Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: Information-Processing Device with Transaction Processor For Executing Subset of Instruction Set Where If Transaction Processor Cannot Efficiently Execute the Instruction It Is Sent to General-Purpose Processor via Interrupt.

Claim Objections

5. Claim 9 is objected to because of the following informalities: Lines 29 to 31 state the following: "executing multiples of specific processes concurrently and achieve efficient execution." There has been a specific process defined prior to this point and the examiner is taking the phrase to mean to refer back to it and not other specific

processes. Also, since the efficiency of the processors is being compared, the qualifier "more" must be inserted. Thus, the examiner is taking the phrase to mean: "executing multiples of a specific process concurrently and achieving more efficient execution."

6. Claims 11 and 12 are objected to because of the following informalities: line 19 states that the "process is judged not by said second processor". This statement makes it unclear as to what the execution of the process is not being judged upon. The examiner is taking the phrase to mean the "process is judged not efficient by said second processor" based on the specification. Claim 12 is objected to because without the insertion of "efficient" in claim 11, it also becomes unclear because there no prior mention of efficiency associated with the instruction. This is remedied with the correction mentioned above.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> **The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.**

8. Claims 1-16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

9. Claim 1 recites the limitation "the entire instruction set" in line 14. There is insufficient antecedent basis for this limitation in the claim. There is no previous mention of an entire instruction set. The examiner is taking the instance "an instruction set" of lines 10-11 to mean an entire instruction set.

10. Claim 9 recites the limitation "the entire instruction set" in line 30. There is insufficient antecedent basis for this limitation in the claim. The examiner is taking the instance "an instruction set" of lines 26-27 to mean an entire instruction set.

Claim Rejections - 35 USC § 102

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

12. Claims 1-4 and 7 are rejected under 35 U.S.C. 102(e) as being anticipated by Evoy (6,330,658).

13. In regard to claim 1, Evoy discloses an information-processing device (figure 2) that executes a specific process more frequently than other processes among a variety of processes; Column 6, lines 10-14 show that 90% of the instructions (Java bytecodes) use ¼ the code of the other 10%. Clearly the process defining ¼ of the code is executed more frequently in order to make up 90% of the instructions; said information-processing device comprising:

a. a first processor (figure 2, element 40) capable of executing an instruction set corresponding to the variety of processes; Column 5, lines 66-67 show that the processor includes an instruction set. Column 6, lines 4-17, show that the processor handles the complex instructions not handled by the slave processor

(the 10%). This means that it can execute the same format of instructions as the slave, which executes the Java bytecodes, and thus its instruction set corresponds to the variety of processes.

b. a second processor (figure 2, element 50) capable of executing a portion of or the entire instruction set, said second processor being capable of executing a part of said instruction set corresponding to the specific process more efficiently than said first processor; Column 6, lines 4-17, show that this slave processor executes 90% of the instruction set, which corresponds to the specific process as shown above. The abstract shows that the second (slave) processor is capable of efficient execution of its Java instructions and the first (master) processor efficient execution of its instructions. Thus the second is more efficient for Java instructions than the first, which has been shown to also be capable of executing Java codes.

c. wherein said second processor executes the specific process whereas said first processor executes the other processes. As shown above, the second processor executes 90% of the instructions and the first processor 10%.

14. In regard to claim 2, Evoy discloses the information-processing device as claimed in claim 1, as shown above, wherein all the processes are allocated to said second processor initially, wherein said second processor passes a given process to said first processor by interrupting said first processor in a case in which an instruction other than the part of the instruction set corresponding to the specific process must be executed. Column 6, lines 14-17, show that the second processor triggers an exception

for the first processor if it cannot handle an instruction. This means it is not in the specific process but in the other processes in the variety of processes as described above. This means that all instructions have been initially sent to the second processor and when deemed not executable, sent to the first. Column 8, line 66- column 9, line 3, show that the exception sent to the first processor is an interrupt.

15. In regard to claim 3, Evoy discloses the information-processing device as claimed in claim 1, as described above, wherein all the processes are allocated to said second processor initially, wherein said second processor passes a given process to said first processor by interrupting said first processor when an instruction that cannot be executed or cannot be efficiently executed by said second processor appears in said given process. Column 6, lines 14-17, show that the second processor triggers an exception for the first processor if it cannot handle an instruction. This means that all instructions have been initially sent to the second processor and when deemed not executable, sent to the first. Column 8, line 66- column 9, line 3, show that the exception sent to the first processor is an interrupt.

16. In regard to claim 4, Evoy discloses the information-processing device as claimed in claim 3, as described above, wherein said instruction that cannot be executed or cannot be efficiently executed by said second processor is a floating-point arithmetic operation. Column 6, lines 27-28, show that it is desirable to have the first (master) processor handle floating point operations. Since all instructions were sent to the second processor and the first processor handles or executes it, then the second processor must not be able to execute it or execute it efficiently.

17. In regard to claim 6, Evoy discloses the information-processing device as claimed in claim 1, as described above, wherein said first processor is a general-purpose processor, wherein said second processor is a transaction processor designed to efficiently execute a transaction process as the specific process. Column 5, lines 66-67, show that the first processor, 40, is a load/store architecture. This architecture is defined to be that of a general-purpose processor by Hennessy on page 191. Column 4, lines 30-38, show that the system downloads substantial program code from a server. This makes for frequent transactions over a network in dealing with platform-independent code such as Java. Since the second processor executes Java code, it must interface over the network and thus is a transaction processor.

18. In regard to claim 7, Evoy discloses the information-processing device as claimed in claim 1, as described above, wherein said first processor and said second processor share a memory space. Figure 2 shows that there is one memory space (element 25) and that each processor (40 and 50) is connected to it using a common bus. Thus the two processors share a memory space.

Claim Rejections - 35 USC § 103

19. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

20. Claims 5 and 8-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Evoy in view of Hennessy.

21. In regard to claim 5,

a. Evoy discloses the information-processing device as claimed in claim 1, as described above, wherein said second processor is capable of executing the part of said instruction set corresponding to the specific process more efficiently than said first processor (as described above)

b. Evoy does not disclose that the second processor executes the specific process more efficiently by executing said specific process in parallel by use of at least one of a multi-threading method and a multi-processing method.

c. Hennessy has disclosed on page 718 in figure 9.2 a multiprocessor for increasing efficiency by parallel processing. It is defined page 712, last paragraph that a parallel processing program is a program that runs on multiple processors, thus the processors run in parallel.

d. Hennessy has taught on page 712 that computers are made more powerful by connecting many small ones or by multiprocessing. It also says that multiprocessors may be faster than the fastest uniprocessor. This notable processing speed increase would have motivated one of ordinary skill in the art to modify the design of Evoy to make the second processor a multiprocessor as taught by Hennessy.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Evoy to make the second processor execute in parallel by making it a multiprocessor as taught by Hennessy so that execution is faster and more efficient.

22. In regard to claim 8,

a. Evoy discloses the information-processing device as claimed in claim 1, as described above,

b. Evoy does not disclose wherein said information-processing device includes a plurality of first processors and second processors.

c. Hennessy has disclosed on page 718 in figure 9.2 a multiprocessor for increasing efficiency by parallel processing.

d. Hennessy has taught on page 712 that computers are made more powerful by connecting many small ones or by multiprocessing. It also says that multiprocessors may be faster than the fastest uniprocessor. This notable processing speed increase would have motivated one of ordinary skill in the art to modify the design of Evoy to make the first and second processors multiprocessors as taught by Hennessy.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Evoy to make the first and second processors multiprocessors as taught by Hennessy so that execution is faster and more powerful.

23. In regard to claim 9,

a. Evoy discloses an information-processing device (figure 2) that executes a specific process more frequently than other processes among a variety of

processes; Column 6, lines 10-14 show that 90% of the instructions (Java bytecodes) use ¼ the code of the other 10%. Clearly the process defining ¼ of the code is executed more frequently in order to make up 90% of the instructions; said information-processing device comprising:

i. a first processor (figure 2, element 40) capable of executing an instruction set corresponding to the variety of processes; Column 5, lines 66-67 show that the processor includes an instruction set. Column 6, lines 4-17, show that the processor handles the complex instructions not handled by the slave processor (the 10%). This means that it can execute the same format of instructions as the slave, which executes the Java bytecodes, and thus its instruction set corresponds to the variety of processes.

ii. a second processor (figure 2, element 50) capable of executing a portion of or the entire instruction set, said second processor being capable of achieving more efficient execution than said first processor; Column 6, lines 4-17, show that this slave processor executes 90% of the instruction set, which corresponds to the specific process as shown above. The abstract shows that the second (slave) processor is capable of efficient execution of its Java instructions and the first (master) processor efficient execution of its instructions. Thus the second is more efficient for Java instructions than the first, which has been shown to also be capable of executing Java codes.

iii. wherein said second processor executes the specific process whereas said first processor executes the other processes. As shown above, the second processor executes 90% of the instructions and the first processor 10%.

b. Evoy does not disclose that the second processor is capable of executing multiples of a specific process concurrently.

c. Hennessy has disclosed on page 718 in figure 9.2 a multiprocessor for increasing efficiency by parallel processing. It is defined page 712, last paragraph that a parallel processing program is a program that runs on multiple processors, thus the processors run in parallel. This means that if applied to the system of Evoy, the process that the second processor executes would be run on multiple processors, or multiples of the process would be executed.

d. Hennessy has taught on page 712 that computers are made more powerful by connecting many small ones or by multiprocessing. It also says that multiprocessors may be faster than the fastest uniprocessor. This notable processing speed increase would have motivated one of ordinary skill in the art to modify the design of Evoy to make the first and second processors multiprocessors as taught by Hennessy.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Evoy to make the first and second processors multiprocessors as taught by Hennessy so that execution is faster and more powerful.

24. In regard to claim 10, Evoy in view of Hennessy discloses the information-processing device as claimed in claim 9, as shown above, wherein all the processes are allocated to said second processor initially, wherein said second processor passes a given process to said first processor in a case in which an instruction other than the part of the instruction set corresponding to the specific process must be executed. Column 6, lines 14-17, show that the second processor triggers an exception for the first processor if it cannot handle an instruction. This means it is not in the specific process but in the other processes in the variety of processes as described above. This means that all instructions have been initially sent to the second processor and when deemed not executable, sent to the first.

25. In regard to claim 11, Evoy in view of Hennessy discloses the information-processing device as claimed in claim 9, as described above, wherein all the processes are allocated to said second processor initially, wherein said second processor passes a given process to said first processor when an instruction that cannot be executed appears or the execution of the process is judged not efficient by said second processor in said given process. Column 6, lines 14-17, show that the second processor triggers an exception for the first processor if it cannot handle an instruction. This means that all instructions have been initially sent to the second processor and when deemed not executable, sent to the first.

26. In regard to claim 12, Evoy in view of Hennessy discloses the information-processing device as claimed in claim 11, as described above, wherein said instruction that cannot be executed or cannot be efficiently executed by said second processor is a

floating-point arithmetic operation. Column 6, lines 27-28, show that it is desirable to have the first (master) processor handle floating point operations. Since all instructions were sent to the second processor and the first processor handles or executes it, then the second processor must not be able to execute it or execute it efficiently.

27. In regard to claim 13,

a. Evoy in view of Hennessy discloses the information-processing device as claimed in claim 9, as described above, wherein said second processor is capable of executing all or part of said instruction set corresponding to the specific process more efficiently than said first processor (as described above)

b. Evoy in view of Hennessy does not disclose that the second processor executes the specific process more efficiently by executing said specific process in parallel by use of at least one of a multi-threading method and a multi-processing method.

c. Hennessy has disclosed on page 718 in figure 9.2 a multiprocessor for increasing efficiency by parallel processing. It is defined page 712, last paragraph that a parallel processing program is a program that runs on multiple processors, thus the processors run in parallel.

d. Hennessy has taught on page 712 that computers are made more powerful by connecting many small ones or by multiprocessing. It also says that multiprocessors may be faster than the fastest uniprocessor. This notable processing speed increase would have motivated one of ordinary skill in the art

to modify the design of Evoy in view of Hennessy to make the second processor a multiprocessor as taught by Hennessy.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Evoy in view of Hennessy to make the second processor execute in parallel by making it a multiprocessor as taught by Hennessy so that execution is faster and more efficient.

28. In regard to claim 14, Evoy in view of Hennessy discloses the information-processing device as claimed in claim 9, as described above, wherein said first processor is a general-purpose processor, wherein said second processor is a transaction processor designed to efficiently execute a transaction process as the specific process. Column 5, lines 66-67, show that the first processor, 40, is a load/store architecture. This architecture is defined to be that of a general-purpose processor by Hennessy on page 191. Column 4, lines 30-38, show that the system downloads substantial program code from a server. This makes for frequent transactions over a network in dealing with platform-independent code such as Java. Since the second processor executes Java code, it must interface over the network and thus is a transaction processor.

29. In regard to claim 15, Evoy in view of Hennessy discloses the information-processing device as claimed in claim 9, as described above, wherein said first processor and said second processor share common memory address space. Figure 2 shows that there is one memory space (element 25) and that each processor (40 and

50) is connected to it using a common bus. Thus the two processors share a memory space.

30. In regard to claim 8,

a. Evoy in view of Hennessy discloses the information-processing device as claimed in claim 1, as described above,

b. Evoy in view of Hennessy does not disclose wherein said information-processing device includes a plurality of first processors and second processors.

c. Hennessy has disclosed on page 718 in figure 9.2 a multiprocessor for increasing efficiency by parallel processing.

d. Hennessy has taught on page 712 that computers are made more powerful by connecting many small ones or by multiprocessing. It also says that multiprocessors may be faster than the fastest uniprocessor. This notable processing speed increase would have motivated one of ordinary skill in the art to modify the design of Evoy in view of Hennessy to make the first and second processors multiprocessors as taught by Hennessy.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Evoy in view of Hennessy to make the first and second processors multiprocessors as taught by Hennessy so that execution is faster and more powerful.

Conclusion

31. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the

claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

32. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following patents are cited to further show the art with respect to coprocessing and transaction processors.

US Pat No 4,991,080 to Emma discloses a coprocessor that preprocesses instructions before sending them to a main processor for further processing.

US Pat No 4,395,758 to Helenius discloses a system that uses an accelerator processor to optimize execution and includes transaction processing.

US Pat No 5,329,626 to Klein discloses a distributed system using a transaction processor.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane F Gerstl whose telephone number is (703)305-7035. The examiner can normally be reached on M-F 6:45-4:15 (First Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703)305-9712. The fax phone number for the organization where this application or proceeding is assigned is (703)872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)305-3900.

Shane F Gerstl

Examiner
Art Unit 2183

SFG
November 20, 2003

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100